

FIG. 1

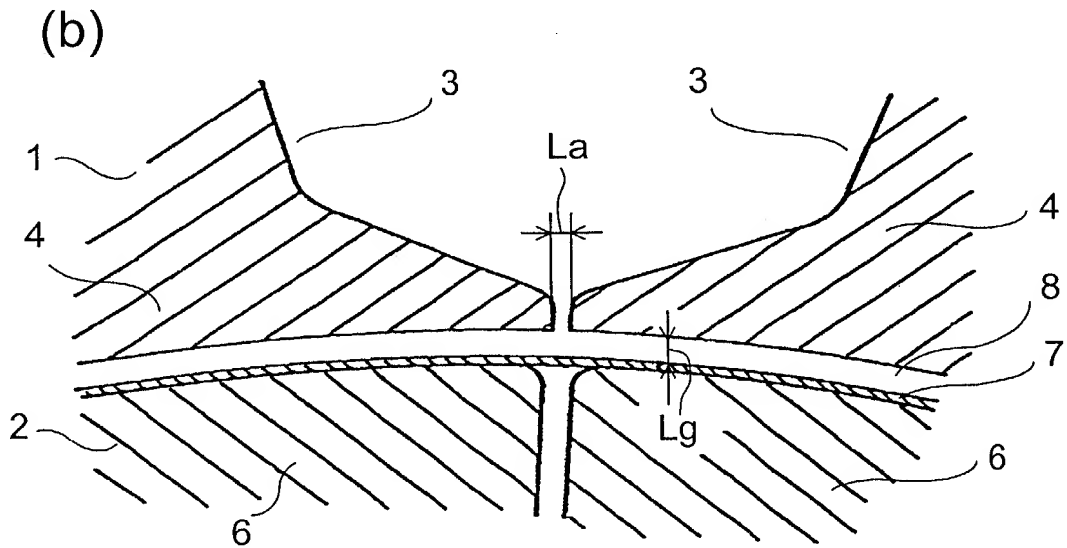
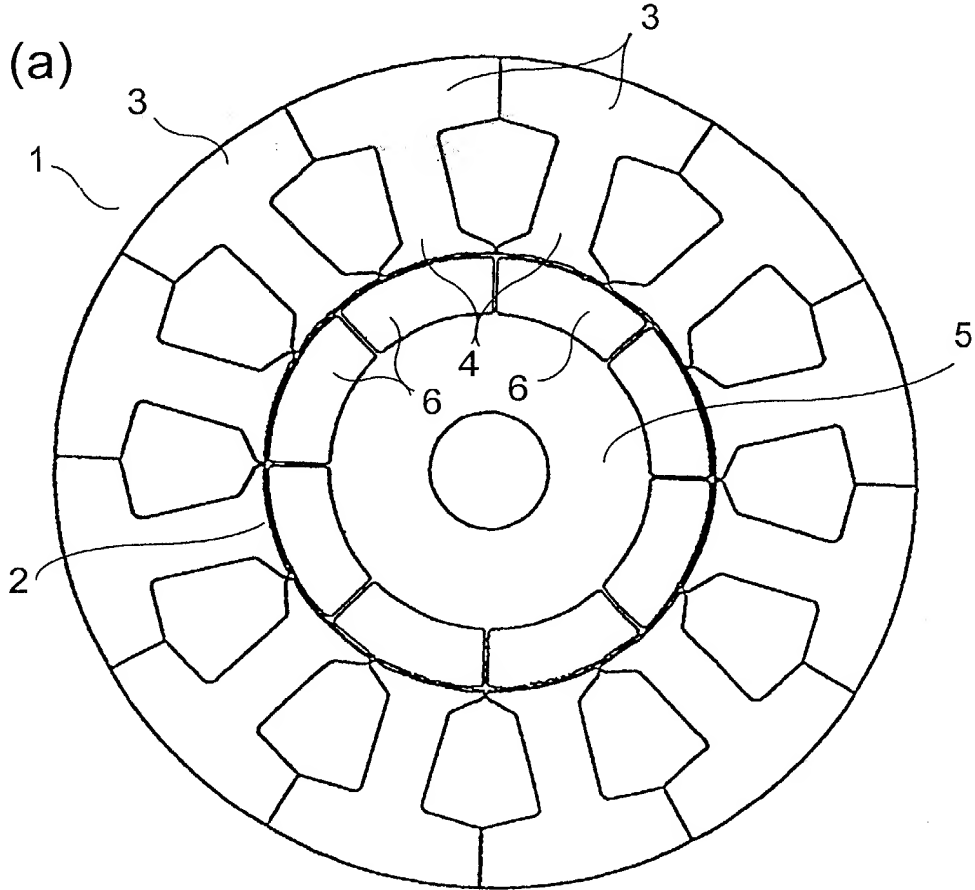


FIG. 2

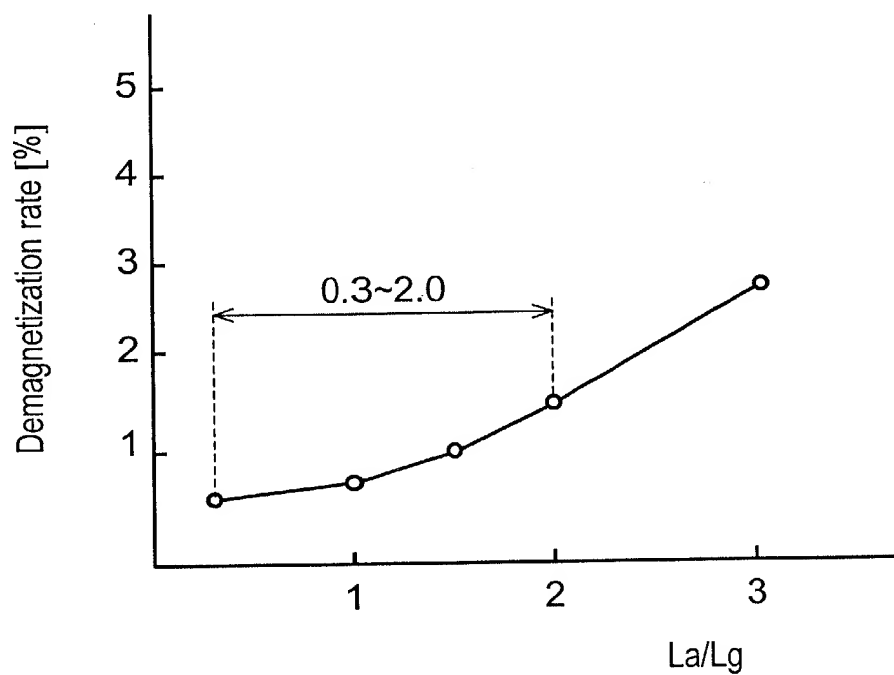


FIG. 3

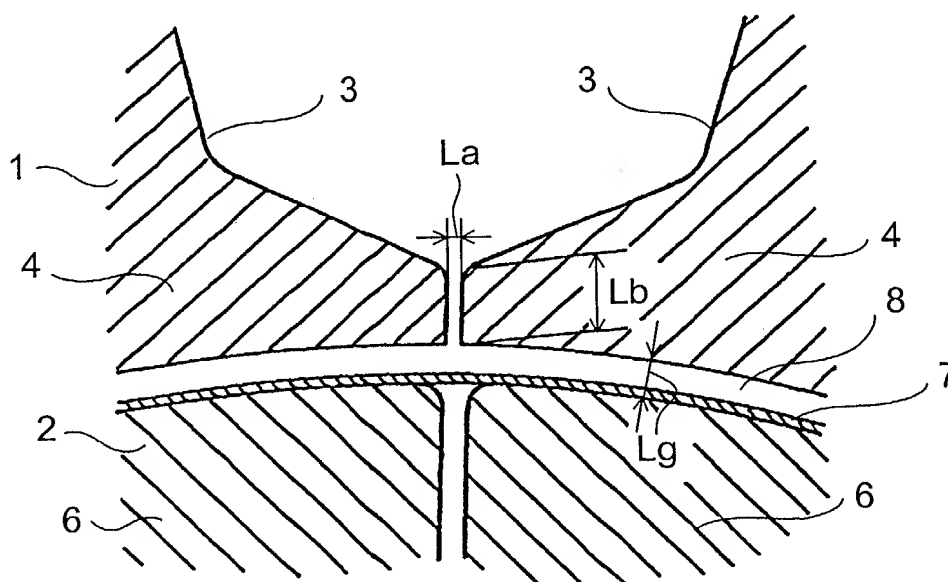
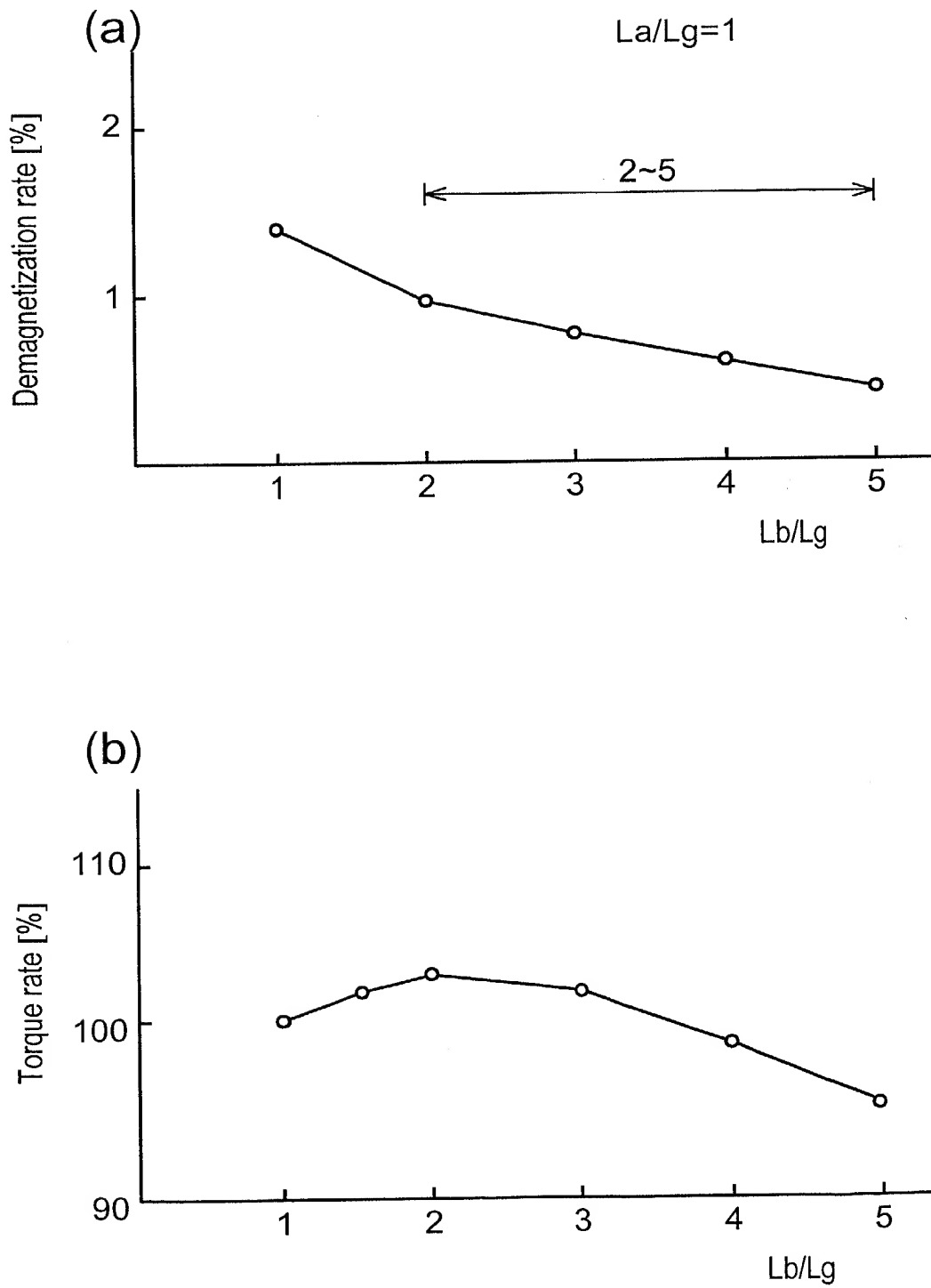


FIG. 4



A schematic cross-sectional diagram of a semiconductor device. The diagram shows a central vertical channel or trench. On either side of this channel are two main regions, each containing a layer labeled '4'. Above these regions are areas labeled '3' and below them are areas labeled '2'. A horizontal layer, possibly a gate oxide, is shown across the middle, with labels 'Lc' and 'Lg' indicating specific thicknesses or positions. Other labels include 'La' at the top of the central channel, 'Lb' near the junction of the central channel and the horizontal layer, and '9' at the bottom of the central channel. The entire structure is surrounded by a substrate material.

FIG. 6

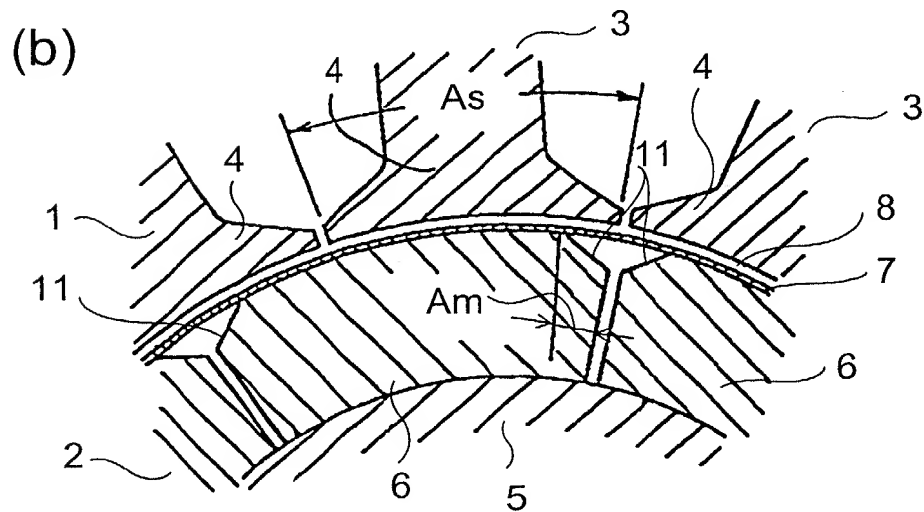
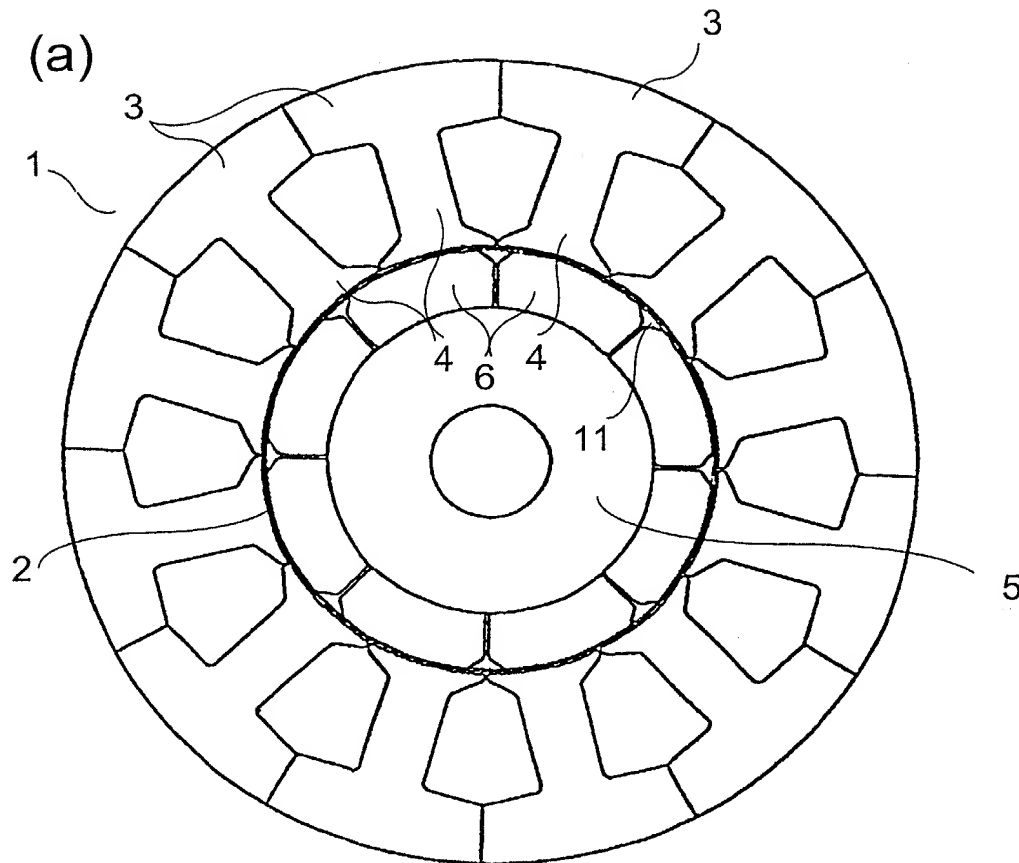


FIG. 7

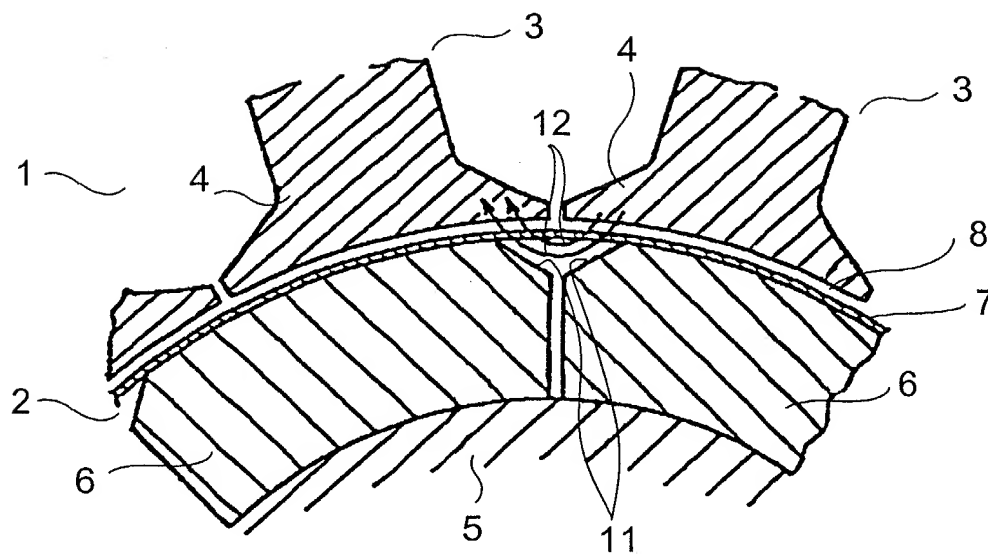


FIG. 8

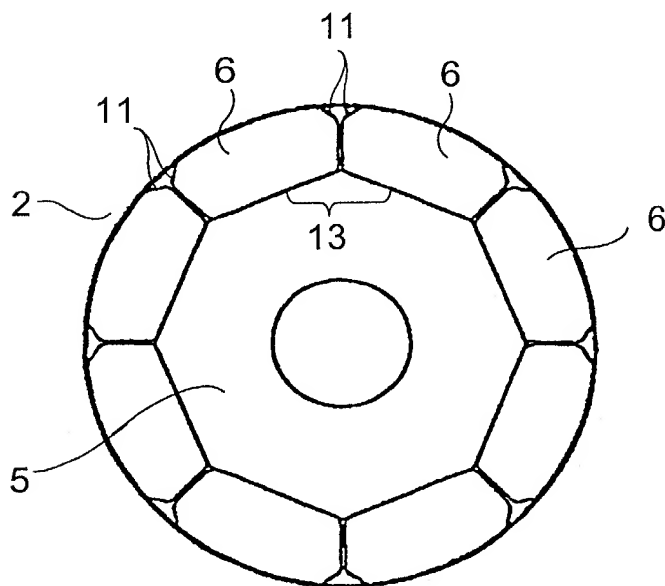


FIG. 9

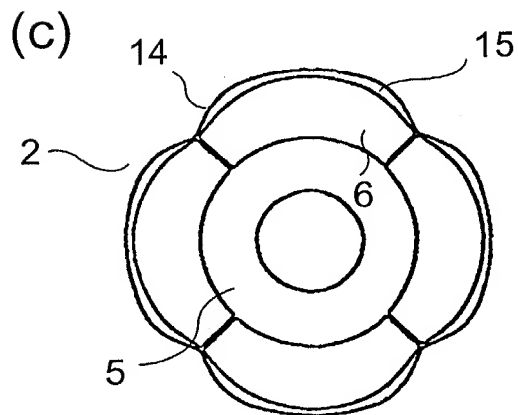
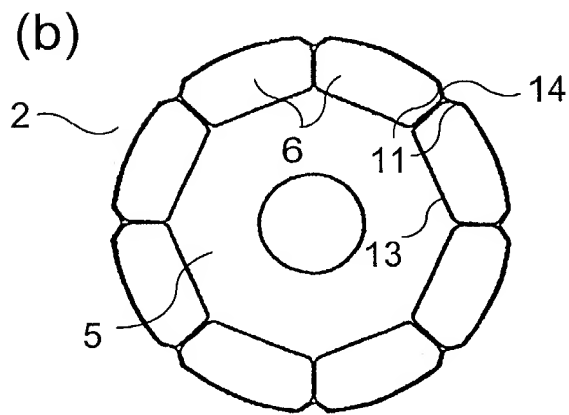
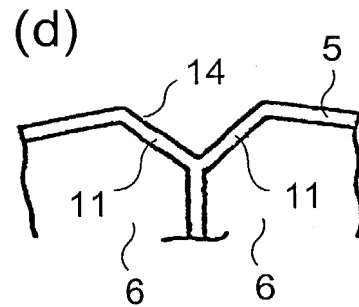
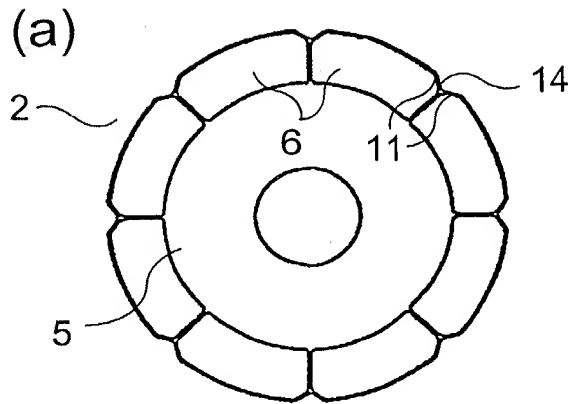


FIG. 10

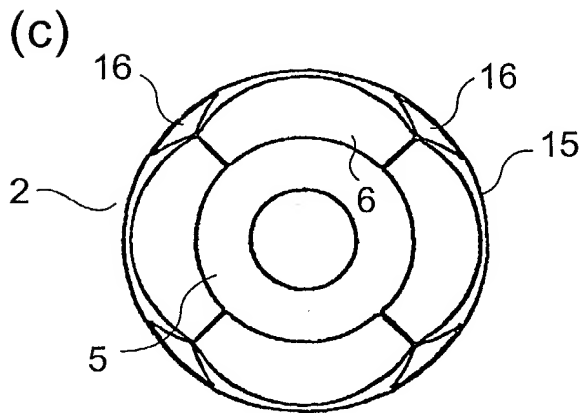
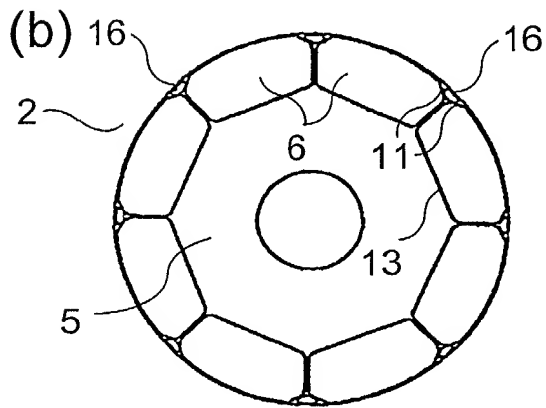
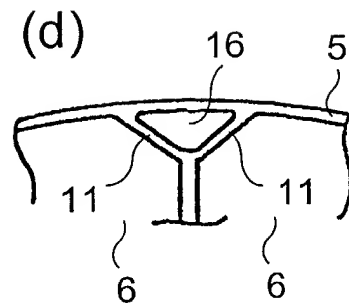
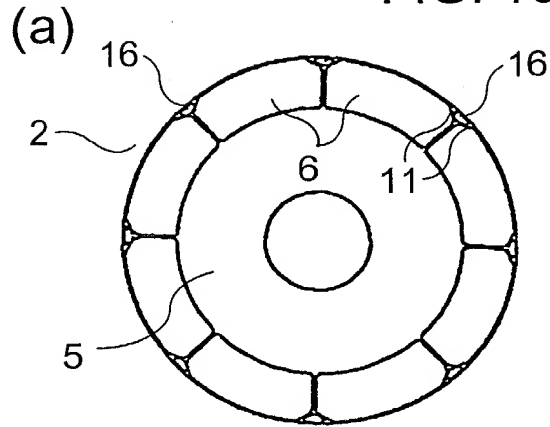




FIG. 11

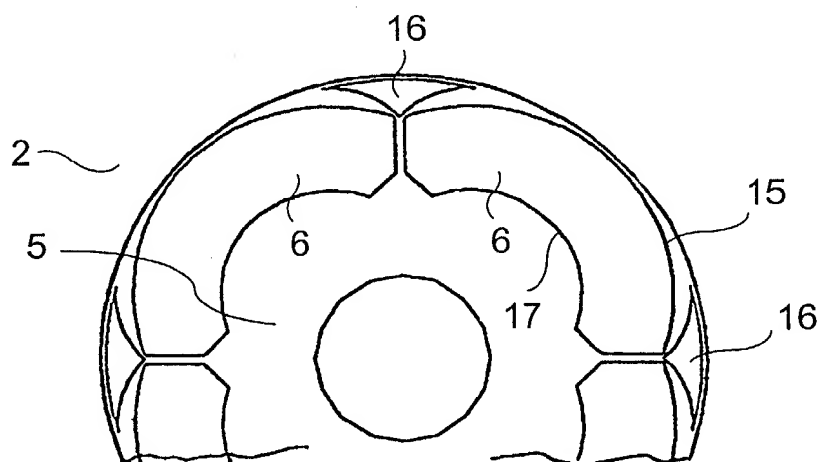


FIG. 12

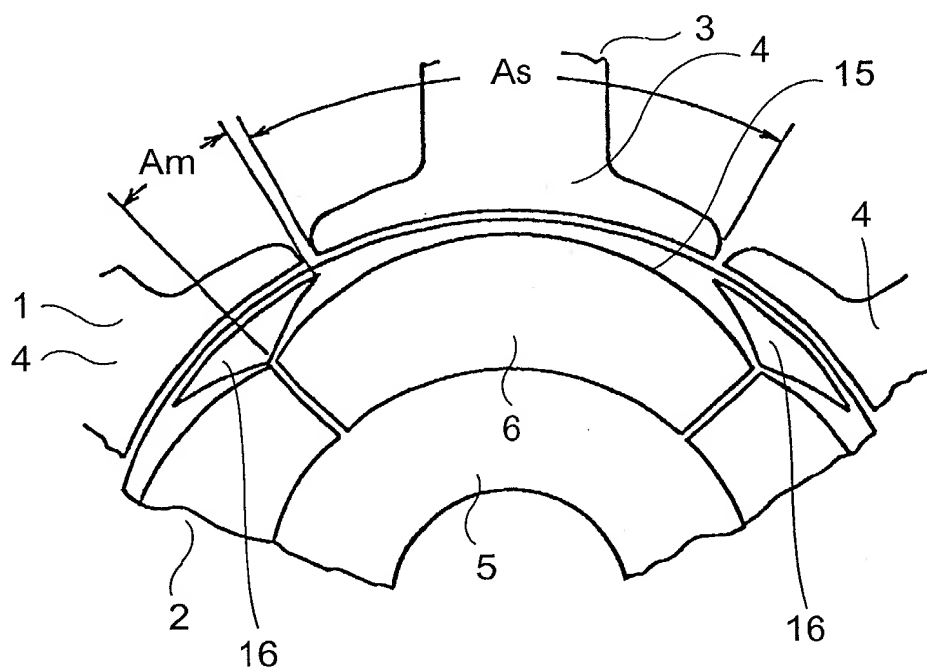


FIG. 13

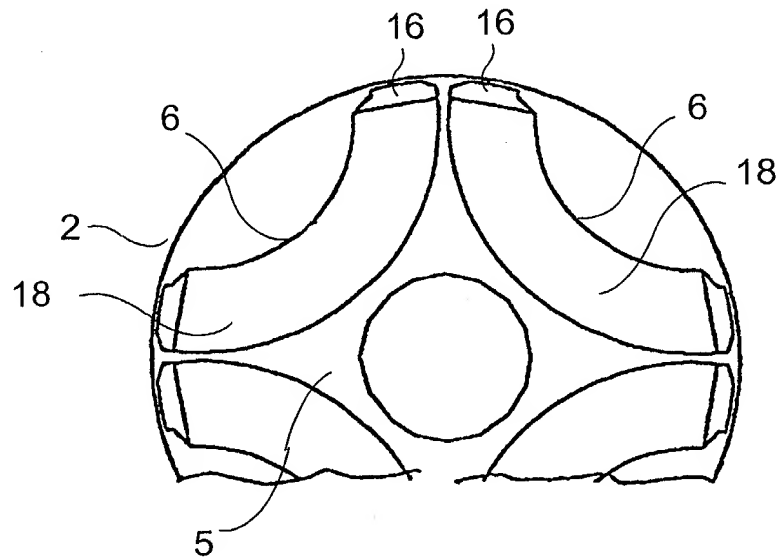


FIG. 14

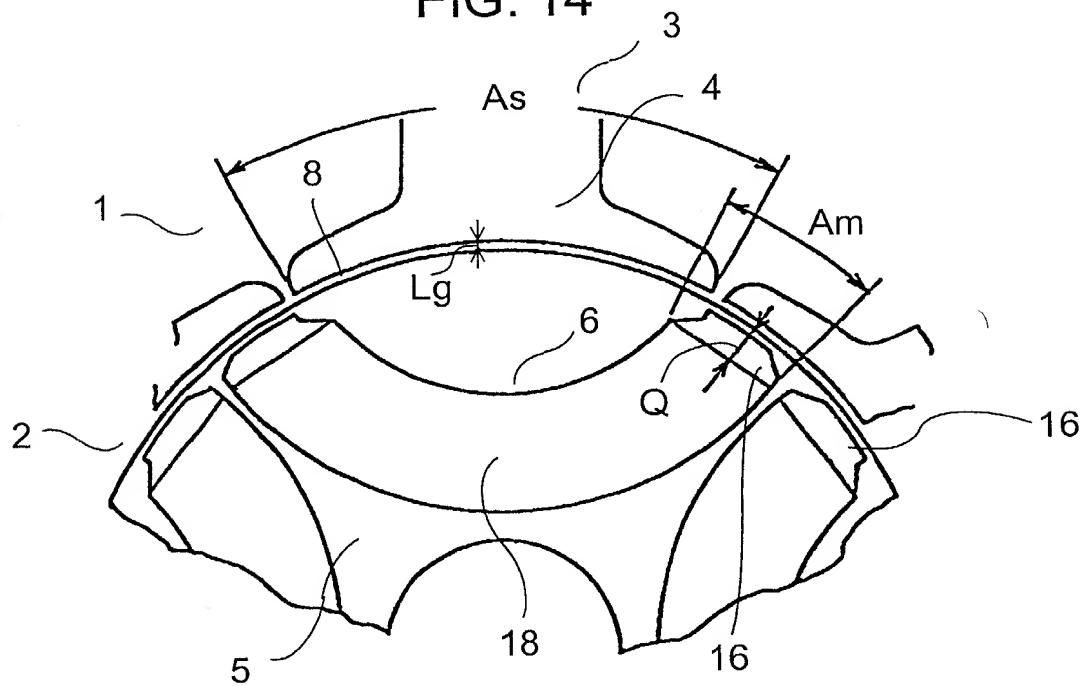


FIG. 15

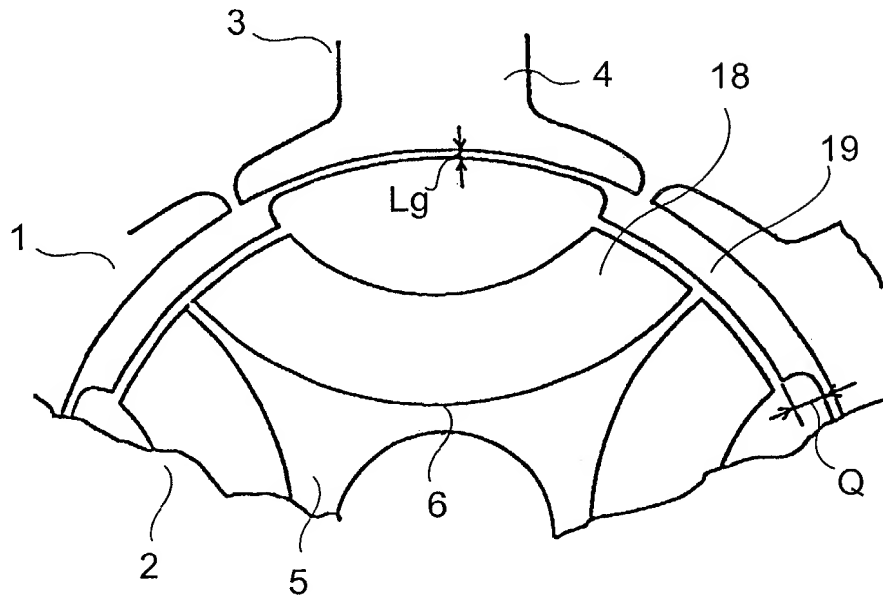


FIG. 16

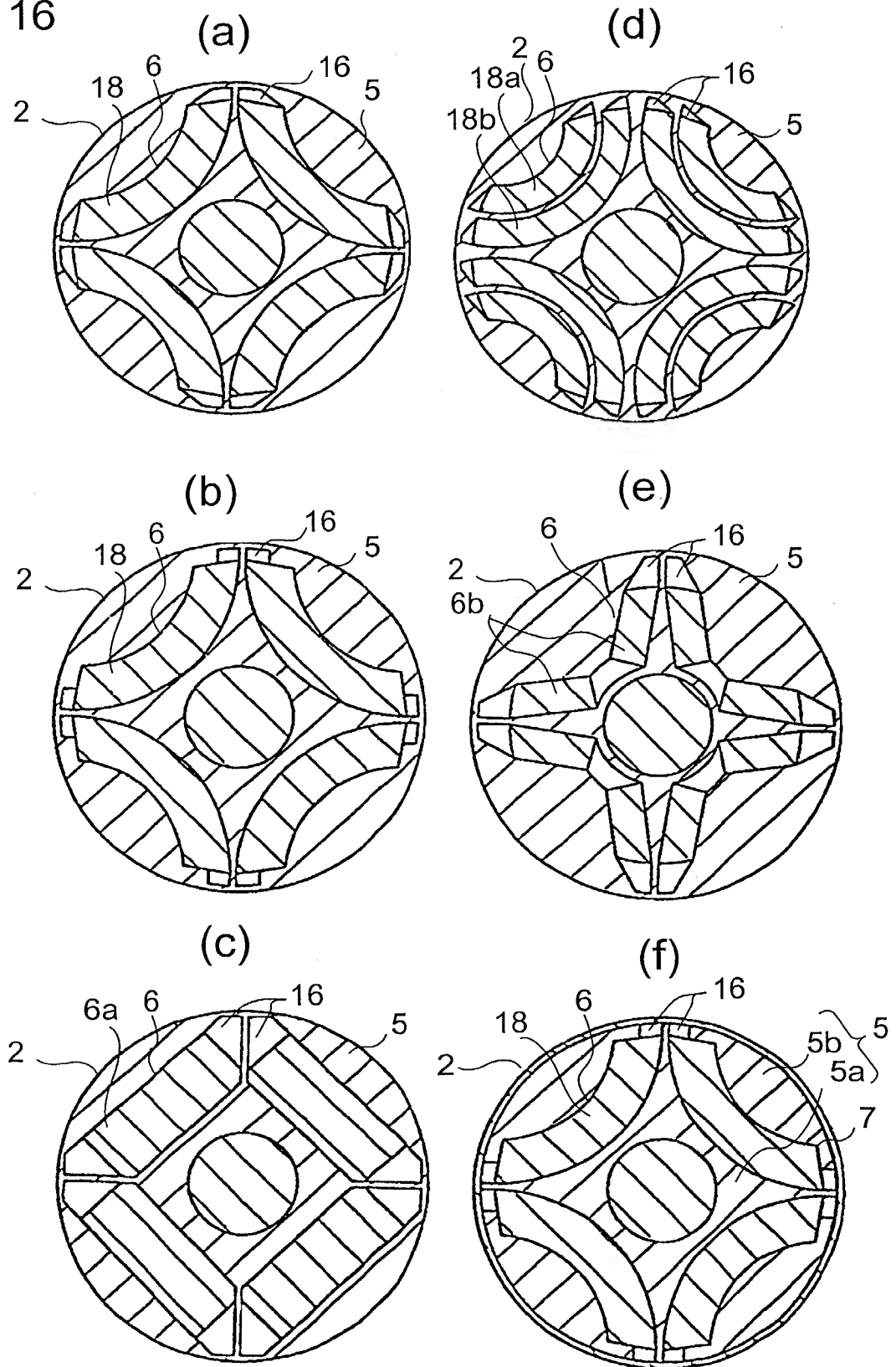
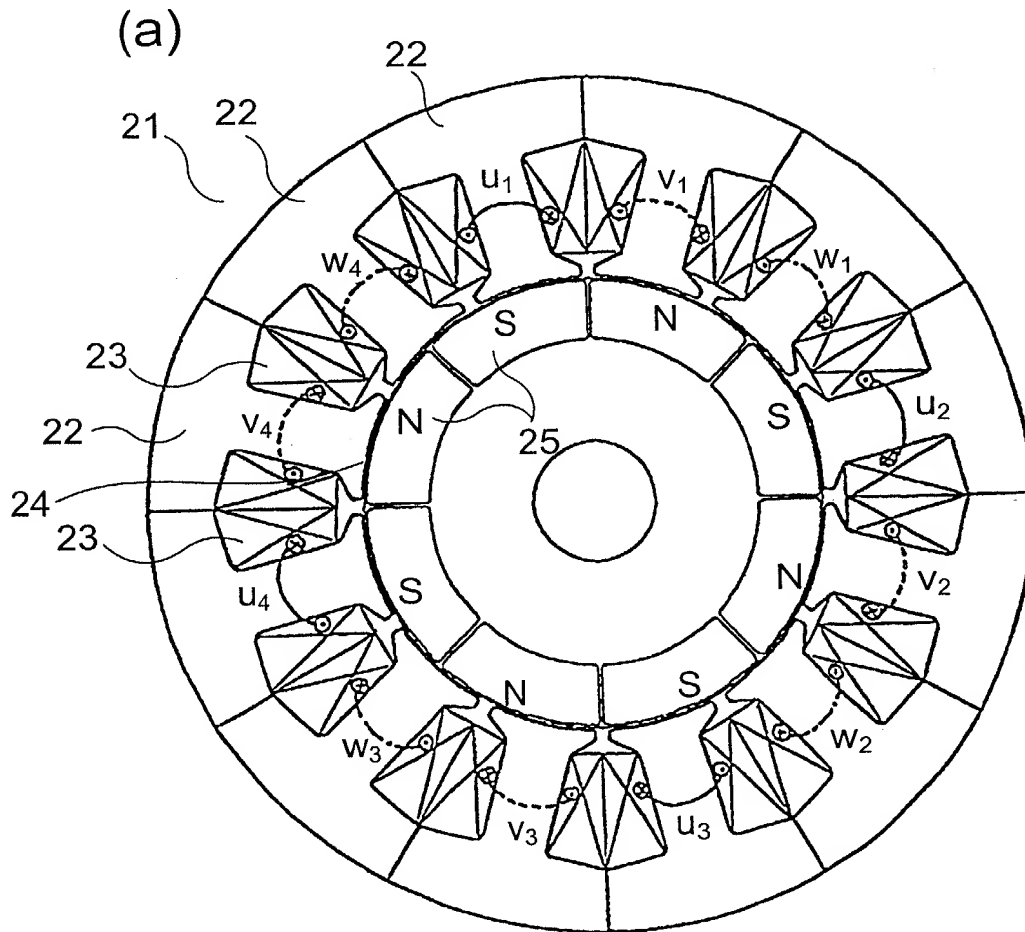


FIG. 17



(b)

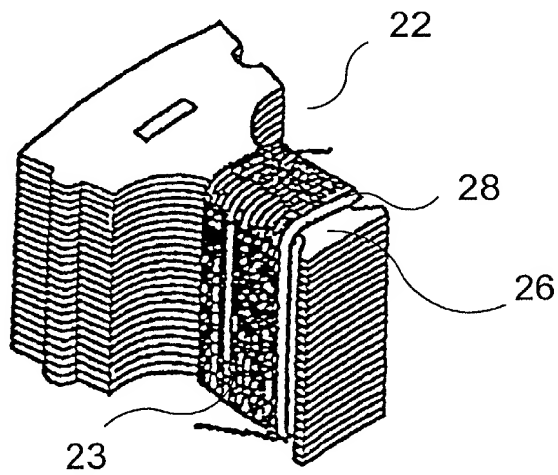


FIG. 18

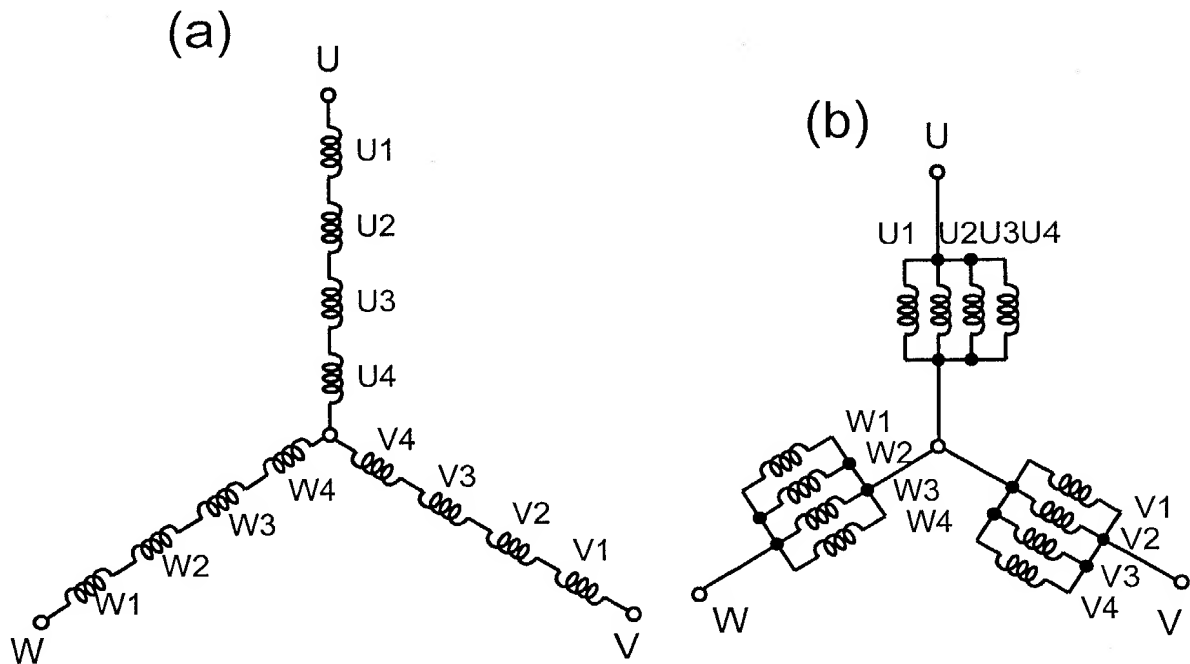


FIG. 19

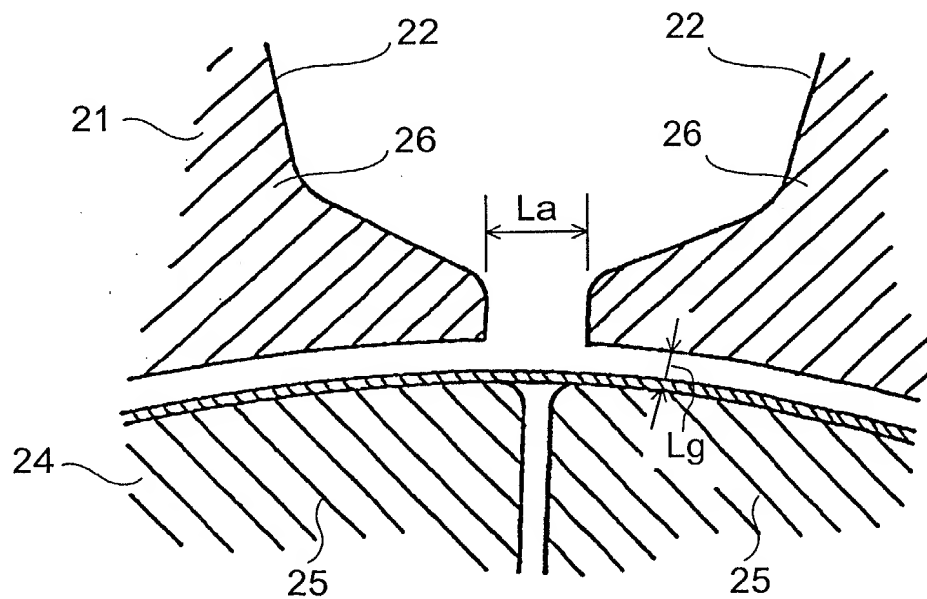


FIG. 20

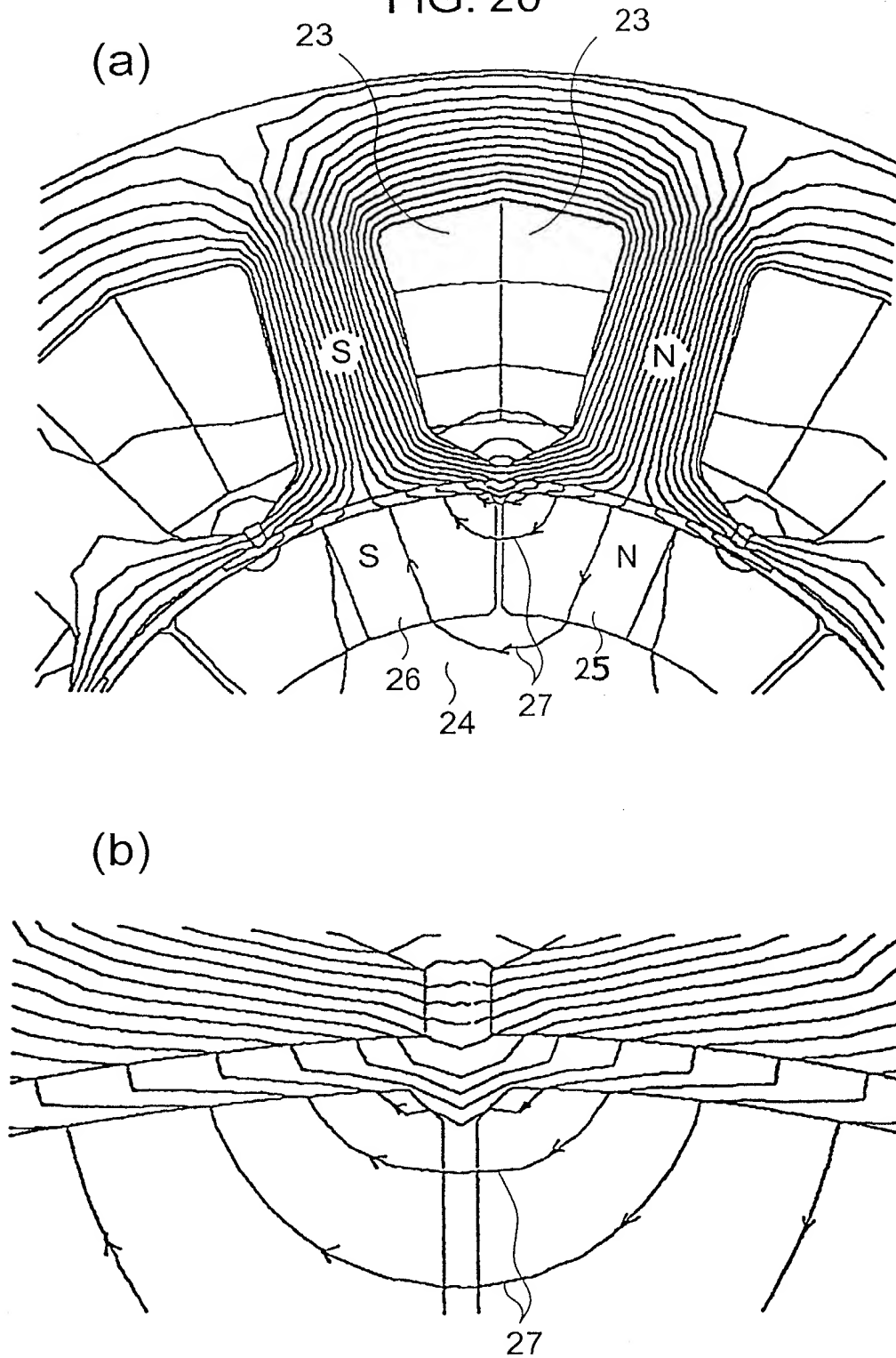


FIG. 21

